

CLAIMS:

1. A data carrier (1) comprising a circuit (2), which circuit (2) comprises the following components, namely

first memory means (5), which are designed for modifiable storage of information (I), the information (I) being modifiable by an ambient parameter of the circuit (2), which ambient parameter acts on the first memory means (5), characterized in that the first memory means (5) comprise a test memory area (7), which is provided for storing test information (TI; TI, TIA, TIB), and

second memory means (16) are provided which are designed for unmodifiable storage of reference information (RI), and

detection means (19) are provided, to which the test information (TI; TI, TIA, TIB) which may be read out from the first memory means (5) and the reference information (RI) which may be read out from the second memory means (16) may be supplied and which are designed, with the aid of the read-out test information (TI; TI, TIA, TIB) and the read-out reference information (RI), to detect a modification of the originally stored test information (TI; TI, TIA, TIB) brought about by an ambient parameter acting on the first memory means (5).

2. A data carrier (1) as claimed in claim 1, characterized in that the detection means (19) comprise comparison means (20) for comparing the stored test information (TI; TI, TIA, TIB) with the stored reference information (RI).

3. A data carrier (1) as claimed in claim 1, characterized in that enabling means (21) are provided for the purpose of irreversibly enabling functioning of the detection means (19), and

the detection means (19) are designed to cooperate with the enabling means (21).

4. A data carrier (1) as claimed in claim 1, characterized in that the detection means (19) are designed to generate and output an indicator signal (DS), which indicator

signal (DS) is provided to indicate a modification of the originally stored test information (TI; TI, TIA, TIB) brought about by an ambient parameter acting on the first memory means (5) and

the circuit (2) is designed to influence its operating behavior as a function of the indicator signal (DS).

5. A data carrier (1) as claimed in claim 1, characterized in that the test information (TI; TI, TIA, TIB) is formed of at least two bits, which at least two bits differ from one another with regard to their logical value.

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6. A circuit (2), which circuit (2) comprises the following components, namely first memory means (5), which are designed for modifiable storage of information (I), the information (I) being modifiable by an ambient parameter of the circuit (2), which ambient parameter acts on the first memory means (5), characterized in that the first memory means (5) comprise a test memory area (7), which is provided for storing test information (TI; TI, TIA, TIB), and

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second memory means (16) are provided which are designed for unmodifiable storage of reference information (RI), and

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detection means (19) are provided, to which the test information (TI; TI, TIA, TIB) which may be read out from the first memory means (5) and the reference information (RI) which may be read out from the second memory means (16) may be supplied and which are designed, with the aid of the read-out test information (TI; TI, TIA, TIB) and the read-out reference information (RI), to detect a modification of the originally stored test information (TI; TI, TIA, TIB) brought about by an ambient parameter acting on the first memory means (5).

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7. A circuit (2) as claimed in claim 6, characterized in that the detection means (19) comprise comparison means (20) for comparing the stored test information (TI; TI, TIA, TIB) with the stored reference information (RI).

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8. A circuit (2) as claimed in claim 6, characterized in that enabling means (21) are provided for the purpose of irreversibly enabling functioning of the detection means (19), and

the detection means (19) are designed to cooperate with the enabling means (21).

9. A circuit (2) as claimed in claim 6, characterized in that the detection means (19) are designed to generate and output an indicator signal (DS), which indicator signal (DS) is provided to indicate a modification of the originally stored test information (TI; TI, TIA, TIB) brought about by an ambient parameter acting on the first memory means (5), and the circuit (2) is designed to influence its operating behavior as a function of the indicator signal (DS).
10. A circuit (2) as claimed in claim 6, characterized in that the test information (TI; TI, TIA, TIB) is formed of at least two bits, which at least two bits differ from one another with regard to their logical value.
11. A circuit (2) as claimed in claim 6, characterized in that the circuit (2) takes the form of an integrated circuit.